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Ramp etc.,) using DAC – change the frequency
Experiment 11 : Write HDL code to simulate Elevator operation

Note : Remove "Table of Content" before including in CP Book

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17ECL58 : Hardware Description Language Lab

A. LABORATORY INFORMATION

1. Lab Overview

Degree:	BE	Program:	EC
Year / Semester :	3/5	Academic Year:	2019-20
Course Title:	Hardware Description Language Lab	Course Code:	15ECL58
Credit / L-T-P:	4 / 0-1-2	SEE Duration:	180 Minutes
Total Contact Hours:	42 Hrs	SEE Marks:	100 Marks
CIA Marks:	40	Assignment	
Course Plan Author:	Narasimha Murthy R	Sign	Dt : 10/08/2019
Checked By:		Sign	Dt : 10/08/2019

2. Lab Content

Unit	Title of the Experiments	Lab	Concept	Blooms
		Hours		Level
1	Write Verilog code to realize all the logic gates	3	Basic gates	L4
			functionali	Analyze
			ty	
2	Write a Verilog program for the following combinational	6	Combinati	L4
	designs		onal logic	
	a. 2 to 4 decoder		circuits	
	b. 8 to 3 (encoder without priority & with priority)		functionali	
	c. 8 to 1 multiplexer.		ty	
	d. 4 bit binary to gray converter			
	e. Multiplexer, de-multiplexer, comparator.			
3	Write a Verilog code to model 32 bit ALU	3	ALU	L4
			functionali	
			ty	

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4		-	g code for the following flip-flops:	3	Flipflops	L4
	SR, D	, JK and T.			functionali	
					ty	
5	-		nary, BCD counters (Synchronous reset and	3	Counters	L4
	-		set) and "any sequence" counters, using		functionali	
	Verilo	g code.			ty	
6	Write	HDL code to	display messages on an alpha numeric LCD	3	LCD	L4
	displa	ıy			Display	
					implement	
					ation	
7	Write	HDL code to	3	Hex	L4	
	code	on seven seg		Keypad		
					implement	
					ation	
8	Write	HDL code to	control speed, direction of DC and Stepper	3	Motor	L4
	moto	r.			implement	
					ation	
9	Write	HDL code to	o accept Analog signal, Temperature sensor	3	Temperatu	L4
			ta on LCD or Seven segment display.		re	
					sensor	
10	Write	HDL code to	generate different waveforms (Sine, Square,	3	ADC	L4
			c.,) using DAC – change the frequency.		implement	
		- /			ation	
11	Write	HDL code to	simulate Elevator operation.	3	Elevator	L4
				_	operation.	

3. Lab Material

Unit	Details	Available
1	Text books	
		In Lib
2	Reference books	
	Lab manual prepared by Department of E & C Engg, SKIT.	In dept
	HDL Programming (VHDL and Verilog)- Nazeih M.Botros- Dreamtech	
	Press (Available through John Wiley - India and Thomson Learning), 2006	
	Edition	
3	Others (Web, Video, Simulation, Notes etc.)	

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		Not Available			

4. Lab Prerequisites:

-	_	Base Course:		-	-
SNo	Course	Course Name	Topic / Description	Sem	Remarks
	Code				
1	17ECL38	Digital Electronics	Knowledge on basic gates	, 3	
			Combinational and Sequential logi	-	
			circuits		

Note: If prerequisites are not taught earlier, GAP in curriculum needs to be addressed. Include in Remarks and implement in B.5.

5. General Instructions

SNo	Instructions	Remarks
1	Observation book and Lab record are compulsory.	
2	Students should report to the concerned lab as per the time table.	
3	After completion of the program, certification of the concerned staff in-	
	charge in the observation book is necessary.	
4	Student should bring a notebook of 100 pages and should enter the readings	
	/observations into the notebook while performing the experiment.	
5	The record of observations along with the detailed experimental procedure of	
	the experiment in the Immediate last session should be submitted and	
	certified staff member in-charge.	
6	Should attempt all problems / assignments given in the list session wise.	
7	It is responsibility to create a separate directory to store all the programs, so	
	that nobody else can read or copy.	
8	When the experiment is completed, should disconnect the setup made by	
	them, and should return all the components/instruments taken for the	
	purpose.	
9	Any damage of the equipment or burn-out components will be viewed	
	seriously either by putting penalty or by dismissing the total group of	
	students from the lab for the semester/year	
10	Completed lab assignments should be submitted in the form of a Lab Record	
	in which you have to write the algorithm, program code along with comments	
	and output for various inputs given	

6. Lab Specific Instructions

SNo	Specific Instructions	Remarks
1	Turn on the computer.	

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2	Double click on Xilinx ISE 12.1 Project Navigator icon.	
3	Select new project in file menu.	
4	Enter the project name and location as shown below and hit Next.	
5	Select the Family, Device, Package and speed as per the requirements and hit	
	Next.	
6	Create a new source by using new source icon or right click on the device/project folder to create new source.	
7	Select the verilog module and enter the file name in New Source Wizard window and hit Next.	
8	Enter the module name - dataflow/behavioral/structural, port name and select the direction. This will create .v source file. Hit Next and finish the initial project creation.	
	Write complete VHDL/Verilog code for implementation and save.	
10	Click on implementation and check for syntax using "Check syntax" option under synthesize tab. If any error, edit and correct VHDL/Verilog code and repeat check syntax until zero errors.	
11	Double click on ISIM simulator by selecting simulation mode to complete the functional simulation of your design.	
12	Click on user constraints and select pre synthesis/post synthesis for assigning the ports, select the ports and save. It will generate .ucf file to source file.	
13	Click on Implement design for checking Place, Route and Map.	
14	Click generate programming file to generate the .bit file for loading into FPGA kit.	
15	Select the COM port and load the bit file to FPGA kit and check the results. Note down the results in observation book.	

B. OBE PARAMETERS

1. Lab / Course Outcomes

#	COs	Teach.	Concept	Instr	Assessment	Blooms'
		Hours		Method	Method	Level
17ECL58.1	Create and verify functionality of	3	Basic gates	Tutorial /	CIA	L2,L3,
	various gates at the different level of		functionali	Demonstr		L4,L5
	abstractions.		ty	atipon/		
				Practical		
17ECL58.2	Design, verify and implement the	6	Combinati	Tutorial /	CIA	L2,L3,
	functionality of various Combinational		onal logic	Demonstr		L4,L5
	logic circuits.		circuits	atipon/		
			functionali	Practical		
			ty			
17ECL58.3	Design and Analyze the functionality of	3	ALU	Tutorial /	CIA	L2,L3,

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32 bit ALU.

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functionali Demonstr

L4,L5

L2,L3, L4,L5

L2,L3, L4,L5

L2,L3, L4,L5

L2,L3, L4,L5

L2,L3, L4,L5

L2,L3, L4,L5

L2,L3,

L4,L5

L2,L3,

L4,L5

-

CIA

CIA

CIA

CIA

CIA

CIA

CIA

CIA

-

atipon/ Practical

-

	52 51071201		runctionan	Demonstr	
			ty	atipon/	
				Practical	
17ECL58.4	Design, verify and implement the	3	Flipflops	Tutorial /	
	functionality of Flipflops.		functionali	Demonstr	
			ty	atipon/	
				Practical	
17ECL58.5	Design, verify and implement the	3	Counters	Tutorial /	
	functionality of counters.		functionali	Demonstr	
			ty	atipon/	
				Practical	
17ECL58.6	Design the digital system for	3	LCD	Tutorial /	
	Interfacing FPGA to alpha numeric LCD		Display	Demonstr	
	display.		implement	atipon/	
			ation	Practical	
17ECL58.7	Design the digital system for	3	Keypad	Tutorial /	
	Interfacing FPGA with Hex Keypad.		implement	Demonstr	
			ation	atipon/	
				Practical	
17ECL58.8	Design the digital system for	3	Motor	Tutorial /	
	Controlling the speed and direction of		implement	Demonstr	
	stepper motor using HDL		ation	atipon/	
				Practical	
17ECL58.9	Design the digital system for	3	Temperatu	Tutorial /	
	Interfacing FPGA with temperature		re	Demonstr	
	sensor		sensor	atipon/	
				Practical	
17ECL58.1	Study of DAC and generation of different	3	ADC	Tutorial /	
0	signals using HDL .		implement	Demonstr	
			ation	atipon/	
				Practical	
17ECL58.1	Design Elevator system.	3	Elevator	Tutorial /	
1			operation.	Demonstr	
1	1		1	/	

Note: Identify a max of 2 Concepts per unit. Write 1 CO per concept.

Total

2. Lab Applications

SNo	Application Area	CO	Level
1	Design of adder and multiplier circuits.		L3
2	Design of PLDs, PLAs, PALs.		L3

42

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3	Desig	gn of 32 bit N	Aicroprocessor and Microcontrollers.			L3		
4	Desig	gn of counter	rs, shift registers.			L3		
5 Design of memory elements L								
6 Design of digital systems.								

Note: Write 1 or 2 applications per CO.

3. Articulation Matrix

(CO – PO MAPPING)

-	Course Outcomes				P	r <mark>og</mark> r	am (Outo	ome	es				
#	COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	Level
17ECL58.1	Create and verify functionality	2	2	3	т 	3		'	0	3	10	• •	3	L4
	of various gates at the different level of abstractions.													
17ECL58.2	Design, verify and implement the functionality of various Combinational logic circuits.		2	3		3				3			3	L4
17ECL58.3	Design and Analyze the functionality of 32 bit ALU.	2	2	3		3				3			3	L4
17ECL58.4	Design, verify and implement the functionality of Flipflops.	2	2	3		3				3			3	L4
17ECL58.5	Design, verify and implement the functionality of counters.	2	2	3		3				3			3	L4
17ECL58.6	Design the digital system for Interfacing FPGA to alpha numeric LCD display.		2	3		3				3			3	L4
17ECL58.7	Design the digital system for Interfacing FPGA with Hex Keypad.		2	3		3				3			3	L4
17ECL58.8	Design the digital system for Controlling the speed and direction of stepper motor using HDL		2	3		3				3			3	L4
17ECL58.9	Design the digital system for Interfacing FPGA with temperature sensor		2	3		3				3			3	L4
17ECL58.10	Study of DAC and generation of different signals using HDL .	2	2	3		3				3			3	L4
17ECL58.11	Design Elevator system.	2	2	3		3				3			3	L4

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15ECL58.	Average											

Note: Mention the mapping strength as 1, 2, or 3

4. Mapping Justification

Марр	lapping Mapping Level		Justification
СО	PO	-	-
CO1	PO1	L4	The basic engineering knowledge is applied for the basic digital integrated circuit coding.
CO1	PO2	L4	Performing experiment allows the easy analysis of problems.
CO1	O1 PO3 L4		Designing a digital system to meet the specific needs within the realistic constraints can be done.
CO1	PO5	L4	Modern tools are used for designing and analysis of systems.
CO1	PO9	L4	Experiments are done in teams to develop team work.
CO1	CO1 PO12 L4		Practical knowledge inculcates inquisitiveness towards continuous learning.
CO2	CO2 PO1 L4		The basic engineering knowledge is applied for the basic digital integrated circuit coding.
CO2	PO2	L4	Performing experiment allows the easy analysis of problems.
CO2	PO3	L4	Designing a digital system to meet the specific needs within the realistic constraints can be done.
CO2	PO5	L4	Modern tools are used for designing and analysis of systems.
CO2	PO9	L4	Experiments are done in teams to develop team work.
CO2	PO12	L4	Practical knowledge inculcates inquisitiveness towards continuous learning.
CO3	PO1	L4	The basic engineering knowledge is applied for the basic digital integrated circuit coding.
CO3	PO2	L4	Performing experiment allows the easy analysis of problems.
CO3	PO3	L4	Designing a digital system to meet the specific needs within the realistic constraints can be done.
CO3	PO5	L4	Modern tools are used for designing and analysis of systems.
CO3	PO9	L4	Experiments are done in teams to develop team work.
CO3	PO12	L4	Practical knowledge inculcates inquisitiveness towards continuous learning.
CO4	PO1	L4	The basic engineering knowledge is applied for the basic digital integrated circuit coding.
CO4	PO2	L4	Performing experiment allows the easy analysis of problems.
CO4	PO3	L4	Designing a digital system to meet the specific needs within the realistic constraints can be done.
CO4	PO5	L4	Modern tools are used for designing and analysis of systems.
	1	1	1

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CO4	cAAS. All rights	L4	Experiments are done in teams to develop team work.
CO4	PO12	 L4	Practical knowledge inculcates inquisitiveness towards continuous
201	1012	_ .	learning.
CO5	PO1	L4	The basic engineering knowledge is applied for the basic digital
			integrated circuit coding.
CO5	PO2	L4	Performing experiment allows the easy analysis of problems.
CO5	PO3	L4	Designing a digital system to meet the specific needs within the
			realistic constraints can be done.
CO5	PO5	L4	Modern tools are used for designing and analysis of systems.
CO5	PO9	L4	Experiments are done in teams to develop team work.
CO5	PO12	L4	Practical knowledge inculcates inquisitiveness towards continuous learning.
CO6	PO1	L4	The basic engineering knowledge is applied for the basic digital
			integrated circuit coding.
CO6	PO2	L4	Performing experiment allows the easy analysis of problems.
CO6	PO3	L4	Designing a digital system to meet the specific needs within the
			realistic constraints can be done.
CO6	PO5	L4	Modern tools are used for designing and analysis of systems.
CO6	PO9	L4	Experiments are done in teams to develop team work.
CO6	PO12	L4	Practical knowledge inculcates inquisitiveness towards continuous
			learning.
C07	PO1	L4	The basic engineering knowledge is applied for the basic digital
			integrated circuit coding.
CO7	PO2	L4	Performing experiment allows the easy analysis of problems.
CO7	PO3	L4	Designing a digital system to meet the specific needs within the
			realistic constraints can be done.
C07	PO5	L4	Modern tools are used for designing and analysis of systems.
C07	PO9	L4	Experiments are done in teams to develop team work.
C07	PO12	L4	Practical knowledge inculcates inquisitiveness towards continuous
			learning.
CO8	PO1	L4	The basic engineering knowledge is applied for the basic digital
			integrated circuit coding.
CO8	PO2	L4	Performing experiment allows the easy analysis of problems.
CO8	PO3	L4	Designing a digital system to meet the specific needs within the
			realistic constraints can be done.
CO8	PO5	L4	Modern tools are used for designing and analysis of systems.
CO8	PO9	L4	Experiments are done in teams to develop team work.
CO8	PO12	L4	Practical knowledge inculcates inquisitiveness towards continuous
			learning.
CO9	PO1	L4	The basic engineering knowledge is applied for the basic digital

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CO9	PO2	L4	Performing experiment allows the easy and	alysis of problems.			
CO9	PO3	L4	Designing a digital system to meet the spe	cific needs within the			
			realistic constraints can be done.				
CO9	PO5	L4	Modern tools are used for designing and a	nalysis of systems.			
CO9	PO9	L4	Experiments are done in teams to develop	team work.			
CO9	PO12	L4	Practical knowledge inculcates inquisitiven	ess towards continuous			
			learning.				
CO10	PO1	L4	The basic engineering knowledge is applie	d for the basic digital			
			integrated circuit coding.				
CO10	PO2	L4	Performing experiment allows the easy and	alysis of problems.			
CO10	PO3	L4	Designing a digital system to meet the spe	cific needs within the			
			realistic constraints can be done.				
CO10	PO5	L4	Modern tools are used for designing and a	nalysis of systems.			
CO10	PO9	L4	Experiments are done in teams to develop	team work.			
CO10	PO12	L4	Practical knowledge inculcates inquisitiven	ulcates inquisitiveness towards continuous			
			learning.				
CO11	PO1	L4	The basic engineering knowledge is applie	d for the basic digital			
			integrated circuit coding.				
CO11	PO2	L4	Performing experiment allows the easy and	alysis of problems.			
CO11	PO3	L4	Designing a digital system to meet the spe	cific needs within the			
			realistic constraints can be done.				
CO11	PO5	L4	Modern tools are used for designing and a	nalysis of systems.			
CO11	PO9	L4	Experiments are done in teams to develop	team work.			
CO11	PO12	L4	Practical knowledge inculcates inquisitiveness towards continuous				
			learning.				

Note: Write justification for each CO-PO mapping.

5. Curricular Gap and Content

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					
3					
4					
5					

Note: Write Gap topics from A.4 and add others also.

6. Content Beyond Syllabus

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
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9	7					
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11 Image: Constraint of the second secon	9					
12	10					
13	11					
14	12					
	13					
15	14					
	15					

Note: Anything not covered above is included here.

C. COURSE ASSESSMENT

1. Course Coverage

Unit	Title	Teachi		No.	of qu	estior	n in Ex	kam		CO	Levels
		ng	CIA-	CIA-	CIA-	Asg-	Asg-	Asg-	SEE		
		Hours	1	2	3	1	2	3			
1	Write Verilog code to realize all	03	1	-	-	-	-	-	1	CO1	L2
	the logic gates										
2	Write a Verilog program for the	03	1	-	-	-	-	-	1	CO2	L3
	following combinational designs										
	a. 2 to 4 decoder										
	b. 8 to 3 (encoder without										
	priority & with priority)										
	c. 8 to 1 multiplexer.										
	d. 4 bit binary to gray converter										
	e. Multiplexer, de-multiplexer,										
	comparator.										
3	Write a Verilog code to model 32	03	1	-	-	-	-	-	1	CO3	L3
	bit ALU										
4	Develop the Verilog code for the	03	1	_	-	-	_	-	1	CO4	L3
	following flip-flops:										
	SR, D, JK and T.										
5	Design a 4 bit binary, BCD	03	1	_	-	-	_	-	1	CO5	L4

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			ous reset and										
			et) and "any										
	sequer		ters, using										
	Verilog												
6		HDL code		03	1	-	-	-	-	-	1	CO6	L4
		-	alpha numeric										
<u> </u>	LCD di	• •											
7			interface Hex	03	1	-	-	-	-	-	1	C07	L4
			y the key code										
	-	en segment o											
8			control speed,	03	-	1	-	-	-	-	1	C08	L4
	directi	on of DC	and Stepper										
	motor.												
9			accept Analog	03	-	1	-	-	-	-	1	CO9	L4
	-	-	re sensor and										
			LCD or Seven										
		nt display.											
10			to generate	03	-	1	-	-	-	-	1	CO10	L4
	differe												
	1 .	-	Ramp etc.,)										
	using	DAC –	change the										
	freque	-											
11		HDL code	to simulate	03	-	1	-	-	-	-	1	CO11	L4
	Elevato	or operation.											
-		Tota	1	42	7	8	5	5	5	5	20	-	-

Note: Write CO based on the theory course.

2. Continuous Internal Assessment (CIA)

Evaluation	Weightage in Marks	СО	Levels
CIA Exam - 1	30	CO1, CO2, CO3, CO4	L23, L3
CIA Exam - 2	30	CO5, CO6, CO7,CO8	L1, L2, L3
CIA Exam - 3	30	CO9,CO10,CO11	L1, L2, L3
Assignment – 1	05	CO1, CO2, CO3, CO4	L2, L3, L4
Assignment – 2	05	CO5, CO6, CO7,CO8	L1, L2, L3
Assignment – 3	05	CO9,CO10,CO11	L1, L2, L3
Seminar – 1	05	CO1, CO2, CO3, CO4	L2, L3, L4
Seminar – 2	05	CO5, CO6, CO7,CO8	L2, L3, L4
Seminar – 3	05	CO9,CO10,CO11	L2, L3, L4

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Other Activities – define			CO1 to CO11	L2, L3, L4		

Other Activities – define		COT to COTT	L2, L3, L4
– Slip test			
Final CIA Marks	40	-	-
-		`	·

SNo	Description	Marks
1	Observation and Weekly Laboratory Activities	05 Marks
2	Record Writing	10 Marks for each Expt
3	Internal Exam Assessment	20 Marks
4	Internal Assessment	5 Marks
5	SEE	600 Marks
-	Total	100 Marks

D. EXPERIMENTS

Experiment 01 : Write Verilog code to realize all the logic gates

-	Experiment No.:	1 Marks		Date Planned	Date Conducte d
1	Title	Write verilog c	ode to realize	e all the logic gate	S
2	Course Outcomes	Create and ve abstractions.	erify function	ality of various g	ates at the different level o
3	Aim	Write Verilog and gate level		ze all the logic g	ates in behavioural, dataflo
4	Material / Equipment Required	Lab Manual			
5	Theory, Formula Principle, Concept		e of program <mark>ogicga</mark>	t	Logical expression and Trut able for all the logic gates.
		_a		c_and d_or	
				e_xor f_not_a	
				g_nand h_nor	
		b		i_xnor	
EC	pared by		ogicga	tes	Checked h



6	Procedure,			• 5	step	l: start								
	Program,	Activity,		• 5	step 2	2: write	prograi	nming						
	Algorithm,	Pseudo			•	3: save t		-						
	Code				-	4: check	-							
				step 5:if error then correct the errorsstep 6:simulate the design										
					-			-	'n					
				step 7: FPGA implementationstep 8: stop										
7	Block,	Circuit,			-	log co	de							
		Diagram,				-		out a.h).					
	Reaction E	quation,		module logicgates(input a,b, outputc_and,d_or,e_xor,f_not_a,g_nand, h_nor,										
	Expected Gr	aph	i xr	_xnor);										
				-		nd= a	& h [.] a	ssian	d_or= a	alb.				
				-				-	not_a=					
				-		and = d		-	not_a–	°α,				
				-	-),						
						or= ~(a D), ∕	_ •	. <u>.</u>					
			ć					Trut	h Tabl	e				
8	Observation	Table,	—	Inj	put				Outpu	ıt				
U	Look-up	Table,		a	b	c_and	d_or	e_xor	f_not_a	g_nand	h_nor	i_xnor		
	Output			0	0	0	0	0	1	1	1	1		
				0	1	0	1	1	1	1	0	0		
				1	0	0	1	1	0	1	0	0		
				1	1	1	1	0	0	0	0	1		
				, т	ruth	table ve	rificatio	<u>.</u> חר	1	1	1	·]		
					uun		mean							
9	Sample Calc	ulations	•	• _										

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10	Graphs, Outputs			-			
		Name	Value	0 ns	200) ns	400 ns
		li a	1				
		16 в	1				
		្រៃ c_and	1				
		lle d_or	1				
		le e_xor	0				
		t_not_a	0				
		1 g_nand	0				
		Lo h_nor	0				
		L _o i_xnor	1				
11	Results & Analysis	• The logic	Gates have	e been realiz	zed and	simulated	using HDL
		codes.					
12	Application Areas	• To write t	he verilog pr	ogram			
13	Remarks						
14	Faculty Signature						
	with Date						

Experiment 02 : Write a Verilog program for the combinational designs

-	Experiment No.:	2	Marks	Date Planned	Date Conducte d
1	Title	Write	a Verilog p	rogram for the combinationa	al designs
2	Course Outcomes		gn, verify a circuits.	nd implement the function	ality of various Combinational
3	Aim		a Verilog p to 4 decode	rogram for the following cor r	nbinational designs
4	Material / Equipment Required	Lab N	Manual		
5	Theory, Formula, Principle, Concept		Boolean E $y0 = \bar{a}$. $y1 = \bar{a}$. y2 = a. y3 = a.	b.en b.en b.en	
6	Procedure, Program, Activity, Algorithm, Pseudo Code		step 2: v step 3: s step 4: c	tart rrite programming ave the program heck syntax error then correct the errors	

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		Circuit, Diagram, on Equation, ed Graph	inp out ass ass ass ass	out a, tput y sign y sign y sign y	b, en $70, y1, y0 = (-7)^{-1} (-7)^$; ,y2,y3 -a) & -a) & & (~ & b &	9; (~b) (b) & e b) & k en;	& en; en; en;				
							th T					
8	Observ	ation			Inpu	1		1	tput		 •	Truth table verification
	Table,	Look-up		en	a	b	y3	y2	y1	y0	•	Truth table vernication
	Table,	-		1	0	0	0	0	0	1		
	,	•		1	0	1	0	0	1	0		
				1	1	0	0	1	0	0		
				1	1 X	1	1	0	0	0		
				<u> </u>		X	0	0	0	0		
9	Sample											
	Calcula	tions										
10	Graphs	, Outputs	Simula	tion \	Wavef	forms			-		_	
			Name				Value		0	ns	 	200 ns 400 ns
			16 4				1				 	
			16 1	b			1					
			د م ^{لل} د م ^{لل}				0 0					
			16,	y1			1					
			1.00	yð			0					
EC												

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11	Results &	Analysis		
12	Applicatio	on Areas	Design of top level digital circuits.	
13	Remarks			
14	Faculty	Signature		
	with Date	2		

-	Experiment No.:	2	Marks	Date Planned		Date Conducte d	
1	Title	Write	a Verilog p	rogram for the combina	ational desig	ns	
2	Course Outcomes	_	ın, verify a circuits.	nd implement the fun	ctionality of	various Co	mbinational
3	Aim			rogram for the followin er without priority)	g combinatio	onal designs	
	Material / Equipment Required Theory, Formula, Principle, Concept			y(2.0)			
	Procedure, Program, Activity, Algorithm, Pseudo Code Block, Circuit,	ma inj ou abe if(step 3: s step 4: c step 5:if FRILO odule enc put [7:0]i ut en; itput reg [ways @(i gin en=1)	write programming ave the program heck syntax error then correct the e mulate the design search from the second search from the second se	rrors		
EC Prei	pared by proved	y< els cat sat sat sat sat sat sat sat sat sat en en	se(i) 500000001 50000001 50000010 5000100 50001000 5000000 5000000 5000000 5000000 5000000 5000000 5000000 5000000 5000000 5000000 50000000 500000000	01:y<=3'b000; 0:y<=3'b001; 0:y<=3'b010; 0:y<=3'b011; 0:y<=3'b100; 0:y<=3'b101; 0:y<=3'b110; 00:y<=3'b111; 0:y<=3'b111; =3'bxxx;		(Checked by

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*8	ANGALORE	Title:													
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	Model	Diagram,													
	Reactio	n Equation,													
		ed Graph													
	Lipeet	ca chaph													
8	Observ	ation	•	Truth	table	verifi	cation								
	Table,	Look-up						Tr	uth Ta	ble					
	Table,	Output		_			Input						Outpu	t	
	,	•	en		i[6]	i[5]	i[4]	i[3]	i[2]	i[1]	i[0]	y[2]	y[1]	y[0]	
			1	X	X	X	X	X	X	X	X	Z	Z	Z	
			0	0	0	0	0	0	0	0	1	0	0	0	
			0	0	0	0	0	0	1	0	0	0	1	0	
			0	0	0	0	0	1	0	0	0	0	1	1	
			0	0	0	0	1	0	0	0	0	1	0	0	
			0	0	0	1	0	0	0	0	0	1	0	1	
			0	0	1	0	0	0	0	0	0	1	1	0	
			0	1	0	0	0	0	0	0	0	1	1	1	
9	Sample														
	Calcula	tions													
10	Graphs	, Outputs	C'		c										
			Simul	ation Wa		is									
			Name		Value	0 ns		200 ns		400 ns	1	600 ns	800	s 	
			la en		0					V	1	\			
			► <mark>117:0</mark> ► 117:0		10000000 111	ZZZ	00000001	00000010	00000100	00001000	X 00010000 X 100	00100000	01000000	10000000	
			Market 1	4	111										
			I		•	•		1		1		1	I	•	
11	Deculte	9 Analysis													
		& Analysis		6											
		tion Areas	Desig	n of top	p level	digita	al circu	lits.							
	Remark														
14	Faculty	Signature													
1.4	racuity	Signature													

-	Experiment No.:	2	Marks	Date Planned	Date Conducte d				
1	Title	Write	Write a Verilog program for the combinational designs						

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2		Design, verify and implement the functionality of v logic circuits.	
3	Aim	Write a Verilog program for the following combination b. 8 to 3 (encoder without priority)	al designs
	Material , Equipment Required	Lab Manual Black Box enc8_3	
5	Theory, Formula Principle, Concept	en	
	Procedure, Program, Activity Algorithm, Pseudo Code		
7	Block, Circuit Model Diagram Reaction Equation Expected Graph		
-	pared by proved	else if (i[2]==1) y=3'b010; else if (i[1]==1) y=3'b001; else if (i[0]==1) y=3'b000; else y=3'b000; end else y=3'b000; end end endmodule	Checked by

Title: Course Lab Manual Page: 20 / 51 copyright 62017. cAAS. All rights reserved. • Truth table verification 8 Observation Table, Look-up Table, Output • Truth table verification 10 0 0 0 0 1 9 Sample Calculations 5 Simulation Waveforms 1 1 10 Graphs, Outputs 5 Simulation Waveforms 1 1 0 9 Sample Calculations 5 Simulation Waveforms 1 1 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 0	SKIT				Teaching Process								Rev	Rev No.: 1.0				
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8 Observation Table, Look-up Table, Output Truth table verification Truth Table Input <	RANGALORE Title:			Со														
Table, Look-up Table, Output Truth Table Truth Table Imput Output Imput Imput Imput Imput Imput Imput Imput Imput Imput Imput Imput Imput	Copyri	ght ©2017.	cAAS. All rights res															
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Image: Source of the product of th		Table,	Look-up															
Imput Output en i7 i6 i5 i4 i3 i2 i1 i0 Y2 Y1 Y0 0 X			-	-							ruth	Table					,	
0 X X X X X X X X X 0 1 0 0 0 1 1 0 0 0 1 1 0 0 1 1 1 0 1					on								÷					
1 0 0 0 0 0 1 0 0 0 1 0 0 0 0 0 1 1 0 0 1 1 0 0 0 0 0 1 1 0 0 1 1 0 0 1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 1 0 0 1 1 1 0 0 1 1 1 0 1 <td></td> <td></td> <td></td> <td>ŀ</td> <td></td>				ŀ														
1 0 0 0 0 1 X X 0 1 0 1 0 0 0 1 X X X 0 1 1 1 0 0 0 1 X X X 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 1 0 0 1 1 1 0 0 1 1 1 0 1 1 1 0 1 <td></td> <td></td> <td></td> <td>ŀ</td> <td></td>				ŀ														
$\frac{1}{1} \begin{array}{ c c c c c c } \hline 0 & 0 & 0 & 0 & 1 & X & X & X & 0 & 1 & 1 \\ \hline 1 & 0 & 0 & 0 & 1 & X & X & X & X & 1 & 0 & 0 \\ \hline 1 & 0 & 0 & 1 & X & X & X & X & X & 1 & 0 & 1 \\ \hline 1 & 0 & 1 & X & X & X & X & X & X & 1 & 1 & 0 \\ \hline 1 & 1 & X & X & X & X & X & X & X & 1 & 1$																		
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1 0 0 1 X X X X X 1 0 1 1 0 1 X X X X X X 1 1 0 1				ŀ														
1 1 X X X X X X 1 1 1 9 Sample Calculations Simulation Waveforms Image: Calculation of the plane				ŀ														
9 Sample Calculations 10 Graphs, Outputs Image: space of the space of t				Ē		0			Х	Х	Х	Х	X	1	1			
Calculations 10 Graphs, Outputs Simulation Waveforms Image: Calculation with the second seco					1	1	X	X	X	X	X	X	X	1	1	1		
12 Application Areas Design of top level digital circuits.		Calcula	tions	Nar	mc 1/2 (7) 1/2 (9) 1/2 (9) 1/2 (9) 1/2 (9) 1/2 (9) 1/2 (9) 1/2 (9) 1/2 (9) 1/2 (9)		Value 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0										2	
12 Application Areas Design of top level digital circuits.	11	Results	& Analysis															
				Desi	gn of	f top	leve	digi	tal ci	rcuits	j.							
13 Remarks						-		-										
14 Faculty Signature	14	Faculty	Signature															
with Date																		

-	Experiment No.:	2	Marks	Date Planned	Conc	ate ducte d			
1	Title	Write	Write a Verilog program for the combinational designs						
2	Course Outcomes	Desig	Design, verify and implement the functionality of various Combinational						

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		logic circuits.
3	Aim	Write a Verilog program for the following combinational designs
		c. 8 to 1 multiplexer.
5	Material / Equipment Required Theory, Formula, Principle, Concept	s[2] s[1] s[0] 1[4] + s[2] s[1] s[0] 1[5] +
	Procedure, Program, Activity, Algorithm, Pseudo Code	 step 3: save the program step 4: check syntax step 5: if error then correct the errors module mux8(i,s,y); In always @(i,s) begin case(s) input [7:0]i; ation case(s)
	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$
8	Observation	Truth table verification
	Table, Look-up	Truth Table
	Table, Output	Input Output
		sel[2] sel[1] sel[0]) Y
		$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$
		$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$
		$\begin{array}{c c c c c c c c c c c c c c c c c c c $
		1 0 1 i[5]
		1 1 0 i[6]
		1 1 1 <i>i</i> [7]
1		

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9	Sample	
	Calculations	
10	Graphs, Outputs	Name Value 0 ns 200 ns 400 ns 500 ns 800 ns Mame Value 0 ns 0 10 010 011 100 111 Mame Value 0 00 001 010 011 100 111 Mame Value 0000 001 010 011 110 111 Mame 1 00000000 00000000 00000000 000100000 001000000 100000000 Mame 1 1 1 1 1 1 1
11	Results & Analysis	
12	Application Areas	Design of top level digital circuits.
13	Remarks	
	Faculty Signature with Date	

-	Experiment No.:	2	Marks		Date Planned		Date Conducte d	
1	Title	Write	a Verilog p	rogram for t	he combina	tional desig	ns	
2	Course Outcomes	-	gn, verify a circuits.	nd impleme	nt the func	tionality of	various C	ombinational
3	Aim	d. 4 l	bit binary to	gray conver	ter			
4	Material / Equipment Required	Lab N	/anual					
5	Theory, Formula, Principle, Concept	G	DLEAN EXPRES 3= B3; 2= B3⊕B2; 1=B2⊕B1; 0=B1⊕B0;	SIONS				
6	Procedure, Program, Activity, Algorithm, Pseudo Code	•	step 2: w step 3: step 4: cl step 5:if step 6:sit	rite progran ave the prog heck syntax error then c mulate the d PGA implem	orrect the en	rrors		
EC Prep	Block, Circuit, bared by proved	i i a a a a	module binary nput [3:0]B; putput [3:0]G; assign G[3]=B assign G[2]=B assign G[1]=B assign G[0]=B endmodule	vtogray(B,G); ; [3]; [3]^B[2]; [2]^B[1];				Checked by

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	Model Diagram,								
	Reaction Equation,								
	Expecte	ed Graph							
8	Observa	ation	Truth tal	ble verificatio	<u></u>				
0	Table,	Look-up			JII				
	Table, (-	INPUT B3 B2 B1 B	OUTPUT 0 G3 G2 G1	G0				
	rubic, v	output	0 0 0 0	0 0 0	0				
			0 0 0 1		1				
			0 0 1 1	0 0 1	0				
			0 1 0 1	0 1 1	1				
			0 1 1 0		1				
			1 0 0 0 1 0 0 1	1 1 0	0				
			1 0 1 0	1 1 1	1				
			$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		0				
			1 1 0 1 1 1 1 0		1				
			1 1 1 1		0				
9	Sample								
	Calcula								
10	Graphs	, Outputs	Simulation W	Vaveforms					
			Name Val	ue 0 ns	200 ns	s	400 ns	600 ns	1800 ns
			▼ 101 ↓ [3] 101	.0 0000	0001 00	11 0010		1010	
			Ալը) օ Ալլլ լ						
			[0] 0 ▼ 📷 G[3:0] 111	.1 (0000)	0001 00	10 0011	(1111	
			L [3] 1 L [2] 1						
			La [1] 1 La [0] 1						
11	Results	& Analysis							
		-	Design of top le	vel digital ci	rcuits.				
-	Remark								
		Signature							
	with Da	-							

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-	Experiment No.:	2	Marks		Date Planned		Date Conducte		
							d		
1	Title			-	or the combina				
2	Course Outcomes	_		and imple	ment the fun	ctionality of	various Co	ombinatio	onal
2	A :	-	ircuits.						
3	Aim		DEMUX						
4	Material / Equipment	Lab Ma	anuai						
	Required								
5	Theory, Formula,		Black Box			Boolean Exp	ression		
1	Principle, Concept		DIACK DUX	demux		-	s1. <u>s0.</u> I. <u>en</u>		
	i incipie, concept				y0 y1		s1. s0. I. en		
				<u></u>	y2 y3		s1. <u>s0. I. en</u> s1. s0. I. en		
				demux	-				
6	Procedure,	•	step 1:	start					
	Program, Activity,	•	-	write prog	ramming				
	Algorithm, Pseudo		-	save the p	•				
	Code	•	-	check synt	-				
		•	-	-	n correct the e	errors			
		•	step 6:s	imulate th	e design				
		•	step 7:	FPGA imple	ementation				
		•	step 8:	stop					
7	Block, Circuit,		le demux(ut s1,s0,I,e	m					
	Model Diagram,		put $y_{3,y_{2,y}}^{y_{3,y_{2,y}}}$						
	Reaction Equation,		F J - ,J ,						
	Expected Graph	-	•	&(~s0)& I&					
				& s0& I& ~ ~s0)& I& ^					
		•	•	s0 & I & ~ei					
		endm			- 3				
		Trut	h Table		-				
8	Observation			I	OUTDUT	 Truth 	table verifi	cation	
	Table, Look-up		INPUT	a0	OUTPUT				
		I	en s1	s0 y3	y2 y1 y0 0 0 1				
EC		1	0 0		$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$				
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App	proved	1	0 1	1 1	0 0 0				
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	Table, (Dutput		
	Sample			
	Calcula	tions		
10	Graphs	, Outputs	Name Val In en 0 In 1 1 In s1 1 In s0 1	lue 0 ns 1200 ns 1400 ns 1
11	Results	& Analysis		
12	Applica	tion Areas	Design of top level digi	ital circuits.
13	Remark	S		
	Faculty with Da	Signature Ite		

-	Experiment No.:	2	Marks		Date Planned	Date Conducte d
1	Title	Write	a Verilog p	rogram for t	he combination	al designs
2	Course Outcomes		gn, verify a circuits.	nd impleme	nt the functior	nality of various Combinational
3	Aim	e. 1:4	4 DEMUX			
4	Material / Equipment Required	Lab N	Manual			
	Theory, Formula, Principle, Concept			mparato ACK BO COMP		
EC Prep	pared by		b(<u>3:0)</u>			Checked by

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6	Procedu Progran Algorith Code Block, Model Reactio	ure, n, Activity, nm, Pseudo	 step 1: start step 2: write programming step 3: save the program step 3: save the program step 4: check syntax step 5: if error then correct the errors step 6: simulate the design module COMP(ntation input [3:0] a,b, output l,e,g); 	
8	Observa	ation	Truth table verification	
	Table,	Look-up	That abe verification	
EC	· usic,	LOOK up		

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	Table, Output	TRUTH TABLE											
					INF	UT				0			
		a3	a2	al	a 0	b3	b2	bl	b0	1	е	g	
		0	0	0	0	0	0	0	0	0	1	0	
		1	0	0	0	0	1	1	1	0	0	1	
		1	0	0	0	1	1	1	1	1	0	0	
		1	0	0	1	1	1	1	1	1	0	0	
		1	1	1	1	1	1	1	1	0	1	0	
9	Sample												
	Calculations												
10	Graphs, Outputs	Name			Value	0	ns		200	ns .		400 ns	60
		▶ 📷	a[3:0]	:	1111 00						1111		
		► 🐝	b[3:0]		0011	0	0\10	11					0011
		16			0								
		ų,	g		1								
11	Results & Analysis												
12	Application Areas	Desigr	n of to	p leve	el digi	tal cir	cuits.						
13	Remarks												
14	Faculty Signature												
	with Date												

Experiment 03 : Write a Verilog code to model 32 bit ALU

-	Experiment No.:	3	Marks		Date Planned		Date Conducte d	
1	Title	Write	e a Verilog co	ode to mo	del 32 bit ALU			
2	Course Outcomes	Desig	gn and Analyz	e the func	tionality of 32 b	it ALU.		
3	Aim	Write	te a Verilog code to model 32 bit ALU					
	Material / Equipment Required	Lab I	Manual					
	Theory, Formula, Principle, Concept		0)	×				
Dror	hared by		alu1				(hecked by



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7	Procedure, Program, Activity, Algorithm, Pseudo Code Block, Circuit, Model Diagram, Reaction Equation, Expected Graph Cobservation Table, Look-up	 step 3: save the program step 4: check syntax step 5: if error then correct the errors module alu(input [3:0] a,b,s, input en, output reg[7:0] y); always@(a, b, s, en, y) begin if(en==1) begin case (s) 4'd0: y=a+b; 4'd1: y=a-b; 4'd2: y=a*b; 4'd2: y=a*b; 4'd2: y=a*b; 4'd3: y={4'd0, ~a}; 4'd4: y={4'd0, (a & b)}; 4'd5: y={4'd0, (a \ b)}; 4'd6: y={4'd0, ~(a \ b)}; 4'd6: y={4'd0, ~(a \ b)}; 4'd9: y={4'd0, ~(a \ b)}; default: y=8'b0000000; endcase end Truth table verification 	
	Table, Look-up	INPUT OUTPUT	
	Table, Output	Operation en S A B Y	
		A+B 1 0000 0111 0010 00001001 A-B 1 0001 0111 0010 00000101	
		A*B 1 0010 0111 0010 00001110	
		Not A 1 0011 0111 0010 11111000	
		A and B 1 0100 0111 0010 00000010 A or B 1 0101 0111 0010 00000111	
		A xor B 1 0110 0111 0010 00000101	
EC		A nand B 1 0111 0110 1111101 A nor B 1 1000 0111 0010 11111000	
-	pared by	A xnor B 1 1001 0111 0010 11111010	cked by
Арр	roved	Any operation 0 S 1001 0111 00000000	

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10		Outputs	Name ► 🙀 p[3:0] ► 🙀 q[3:0] ► 🙀 s[3:0] T en ► 🕞 y[7:0]	Value 0111 0010 0101 1 00000111		10 ns 00001	20 ns 0010	30 ns 0111 0010 0011	40 ns	50 ns 0101	60 ns 0110 00000101
		& Analysis									
			Design of to	op level o	ligit	al circuit	s.				
	Remark										
		Signature									
	with Da	te									

Experiment 04 : Develop the Verilog code for the following flip-flops: SR, D, JK and T.

-	Experiment No.:	4	Marks	Date Planned	Date Conducte d						
1	Title	Deve SR	velop the Verilog code for the SR flip-flop.								
2	Course Outcomes	Desig	Design, verify and implement the functionality of Flipflops.								
3	Aim		lop the Veri), JK and T.	og code for the following	flip-flops:						
4	Material / Equipment	Lab N	Manual								



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	Require	u Formula,			
	-	e, Concept			
		c, concept			
	Procedu		• step 1: start		
	-	n, Activity,	• step 2: write the progr		
	-	ım, Pseudo	 step 3: save the progra 	am	
	Code		 step 4: check syntax step 5: if error then con 	ract the errors	
			 step 5:if error then con module srff(
			input clk,rst,	ion	
			input [1:0]SR, output reg q, qb);		
7	Block,	Circuit,	always@(posedge clk or posedge	ret	
	Model	Diagram,	begin	150	
	Reactio	n Equation,	if(rst==1) begin		
	Expecte	d Graph	$q=1$ 'b0; $qb=\sim q$; end else		
			begin		
			case (SR) 2'b01:begin		
			q = 1'b0;qb = 1'b1; end 2'b10:begin		
			q = 1'b1; qb = 1'b0; end		
			2'b11:begin q = 1'b1;qb = 1'b1; end		
			default: begin end		
			endcase end		
			end endmodule		
			endinotate		
8	Observa		Truth table verification		
	Table,	-	Truth Table		
	Table, C	Jutput	rst SR Q QI		
			1 XX 0 1		
			0 00 Q Q		
			0 0 1 0 1		
			0 1 0 1 0		
			0 1 1 1 1		
L					

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9	Sample							
	Calculations							
10	Graphs, Outputs							
		Name	Value	0 ns		50 ns	100 ns	150 ns
		lie s	0					
		lle r	0					
		U rst	0				mm	
		lle q	0					
		Ug qb	1					
1.1								
	Results & Analysis		al diaital air	i+	c			
	Application Areas Remarks	Design of top lev	ei digitai Cir	cuit	5.			
	Faculty Signature							
	with Date							

-	Experiment No.:	4	Marks		Date Planned	Date Conducte d		
1	Title	Deve JK Fl	•	log code foi	the following f	ip-flop:		
2	Course Outcomes	Desig	gn, verify an	id implemer	it the functional	ity of Flipflops.		
3			lop the Veri), JK and T.	log code foi	the following f	ip-flops:		
4	Material / Equipment Required	Lab N	Manual					
5	Theory, Formula, Principle, Concept	jk(Black Box JK_FF	<u> </u>				
EC			nt	dp				
Pre	pared by		JK_FF				Checked	by



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6 Procedure, Program, Activity, Algorithm, Pseudo Code • step 1: start • step 2: write the program • step 3: save the program • step 4: check syntax							
Program, Activity, Algorithm, Pseudo• step 2: write the program• step 3: save the program							
Program, Activity, Algorithm, Pseudo• step 2: write the program• step 3: save the program							
Program, Activity, Algorithm, Pseudo• step 2: write the program• step 3: save the program							
Program, Activity, Algorithm, Pseudo• step 2: write the program• step 3: save the program							
Algorithm, Pseudo • step 3: save the program	-						
code step 4. check syntax							
step 5:if error then correct the errors							
 step 5.11 error their correct the errors step 6:simulate the design 							
step 0.similate the design step 7: FPGA implementation							
step 7: Frida implementation step 8: stop							
7 Block, Circuit, module jk_ff(
input [1:0] jk,							
J input ist, eik,							
always@(posedge clk,posedge rst)							
Expected Graph begin if(rst==1)							
begin q=1'b0; qb= \sim q; end							
else							
begin case (jk)							
2'b01:q=1'b0;							
2'd10:q=1'b1; 2'b11:q=~q;							
default: begin end							
endcase $qb = \sim q;$							
end							
end endmodule							
enamodule							
2 Observation Truth table configuration							
8 Observation • Truth table verification							
Table, Look-up Table Output Truth Table							
Table, Output							
rst J K Q Qb							
1 XX 0 1							
0 00 Q Qb							
0 01 0 1							
0 1 0 1 0							
0 1 1 Toggle							
0 Sample							
9 Sample Calculations							
Calculations							

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	ight ©2017. cAAS. All rights res Graphs, Outputs	Name	Value	0 ns	200 ns	400 1	ns ,
		🕨 📑 jk[1:0]	00	00	01 10 11		
		Ug rst	0				
		Ug cik	1			INN	
		Ան։ գ	0				
		ပြ _{စ်} qb	1				
11	Deculto 8 Analysia						
	Results & Analysis						
12	Application Areas	Design of top leve	el digital cir	cuits.			
13	Remarks						
14	Faculty Signature						
	with Date						

-	Experiment No.:	4	Marks		Date Planned	Date Conducte d			
1			op the Veri JK and T.	log code for	the following	flip-flops:			
2	Course Outcomes	Desig	n, verify an	d implemen	t the functiona	lity of Flipflops.			
3	Aim	Develo D FF	evelop the Verilog code for the following flip-flop: FF						
4	Material / Equipment Required	Lab M	anual						
5	Theory, Formula, Principle, Concept	d rst	Black Box dff st dff						
6	Procedure, Program, Activity, Algorithm, Pseudo Code		step 3: s step 4: c step 5:if step 6:si	rite the prog ave the prog heck syntax error then c mulate the c PGA implem	ram orrect the errc lesign	rs			
7	Block, Circuit, Model Diagram,		-						

(North Control of the second		SKIT	Teaching Process	Rev No.: 1.0				
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		AAS. All rights rese	rved.					
		n Equation,	• –					
		ed Graph						
8	Observa		Truth table verification					
	Table,	Look-up						
	Table, (Dutput						
9	Sample		module dff(
	Calcula	tions	input d,clk,rst,					
			output q,qb);					
			reg q,qb;					
			always@(posedge clk,posedge rst)					
			begin					
			if (rst=1)					
			begin q=0; qb= \sim q; end					
			else					
			begin q=d; qb=~q; end end					
			endmodule					
			enamodule					
10	Granhs	, Outputs						
11	Results	& Analysis	Name Value 0 ns 200 ns	600 ns				
				┢╋╧┑┙╘╋╺╧┥┛╘┥				
			1 I					
12	Applica	tion Areas	Design of top level digital circuits.					
	Remark		- • •					
		Signature						
	· ·	te						

-	Experiment No.:	4	Marks		nte nned	Date Conducte d	
1	Title	Develo T FF.	p the Veri	og code for the fo	llowing flip-flop	s:	
2	Course Outcomes	Design	, verify an	d implement the f	unctionality of Fl	ipflops.	
3			evelop the Verilog code for the following flip-flops: R, D, JK and T.				
4	Material /	Lab Ma	inual				

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	Equipm Require		tflfp							
		ry, Formula,								
	-	e, Concept								
		-,	rst							
			tflfp							
6	6 Procedure, • step 1: start									
		n, Activity,								
	-	nm, Pseudo								
	Code		 step 3: step 4: check syntax 							
			step 5:if error then correct the errors							
			module tff(t,clk,rst,q,qb);							
			input t,clk,rst; entation							
_		output q,qb;								
7	Block, Model	Circuit,	reg q,qb; always@(posed	lae alk noseda	e ret)					
		Diagram, n Equation,	begin	ige eik,poseug	c 15()					
		ed Graph	if (rst==1)							
			begin q=0;qb= \sim q; end							
			else if(t==1) begin							
				$qb = \sim q; end$						
	end									
		endmodule								
				Truth 7	Fable					
8	Observ	ation	-		1		Truth tabl	e verification		
	Table,	Look-up	rst	Т	Q	Qb				
	Table, (Output	1	X	0	1				
			0	0	Q	Qb				
			0							
			0 1 Toggle							

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9 9	Sample								
Calculations									
10	Graphs, O	, Outputs	Name	Value	0 ns 200 ns	400 ns 60			
			la t	0					
			🔚 clk	0					
			1 rst	1					
			પદિ વ	0					
			🗓 qb	1					
11 F	Results &	Analysis							
12	Applicatio	on Areas I	Design of top level digital circuits.						
13 F	Remarks								
14 F	Faculty S	Signature							
\ \	with Date								

Experiment 05 : Design a 4 bit binary, BCD counters (Synchronous reset and Asynchronous reset) and "any sequence" counters, using Verilog code.

-	Experiment No.:	5	Marks		Date		Date		
					Planned		Conducte		
1	Title	Desig	ın a 4 hit hi	inary counte	rs (Synchror	nous reset a	d nd Asynchro	nous reset)	
		Design a 4 bit binary counters (Synchronous reset and Asynchronous reset) and "any sequence" counters, using Verilog code.							
2	Course Outcomes		Design, verify and implement the functionality of counters.						
-	Aim								
		reset)	reset) and "any sequence" counters, using Verilog code.						
4	Material /	Lab M	Ianual						
	Equipment								
	Required								
5	Theory, Formula,								
	Principle, Concept								
6	Procedure,	•	step 1: s						
	Program, Activity,		-	rite the pro	-				
	Algorithm, Pseudo Code	•	-	ave the prog	ram				
	Code		-	heck syntax error then c	orract the e	rors			
			-	mulate the c		1013			
		•	•	PGA implem	-				
		•	step 8: s						
7	Block, Circuit,	•	_	-					
	Model Diagram,	•	-						

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	Reaction Equation,	• _
	Expected Graph	
8	Observation	Truth table verification
	Table, Look-up	
	Table, Output	
9	Sample	
	Calculations	
10	Graphs, Outputs	
11	Results & Analysis	
12	Application Areas	Design of top level digital circuits.
13	Remarks	
14	Faculty Signature	
	with Date	

_	Experiment No.:	5	Marks		Date Planned		Date Conducte d	
1	Title		-	•	counters (Synd unters, using			ynchronous
2	Course Outcomes	Desig	gn, verify ar	nd implemen	t the function	ality of cou	nters.	
3	Aim			•	counters (Syno unters, using			ynchronous
4	Material / Equipment Required Theory, Formula, Principle, Concept		binarycount	<u>q(3</u> :0)				
6	Procedure, Program, Activity, Algorithm, Pseudo Code		step 1: s step 2: v step 3: s step 4: c step 5: if step 6: s	vrite the prog ave the prog check syntax error then c mulate the c PGA implem	gram orrect the err lesign	ors		

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		iagram,			
	eaction Ec	-			
	pected G	-			
		Тарп	module binarycounter(input clk, clr,dir, output[3:0] q); reg [3:0] count; always @(posedge clk or posedge clr) begin if(clr) count <= 4'h0; else if (dir)	count <= count - 4 else count <= count + 4 end assign q = count; endmodule	
Та	bservation able, L able, Outp	ook-up	Truth table verification clk dir=0 dir=1 q q q 1 0000 1111 1 0001 1110 1 0010 1101 1 0010 1101 1 0010 1011 1 0101 1000 1 0101 1010 1 0101 1010 1 0110 1001 1 0111 1000 1 1010 0111 1 0111 1000 1 1000 0111 1 1010 0101 1 1010 0101 1 1010 0101 1 1010 0101 1 1100 0011 1 1100 0010 1 1110 0000 1 1111 00000 0 00000 1111		
	ample				
	alculation	S			

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10	Graphs	, Outputs	Name	Value	0 ns	20 ns	40 ns	6	0 ns	80 ns	100 ns 120 r	
			1 dir	1								
			Ug cir	0								
			∐ ₀ dk	0								
			V 📲 q[3:0]	1011	0	110 (1101 (1100 / 10	11 X 11D	0 / 1101 /	1110 / 1111 /	0000	
			Ug [3]	1			_					
			16 (2) 16 (1)	0								
			70	/bin_tb/q[1]								
			le clk_period	10000 ps				100	00 ps			
					1							
11	Results	& Analysis										
12	Applica	tion Areas	Design of	top level	digital ci	rcuits.						
13	Remark	S										
14	Faculty	Signature										
	with Da	te										

-	Experiment No.:	5	Marks		Date Planned		Date Conducte d	
1	Title	-			s (Synchrono , using Verilo		id Asynchro	onous reset)
2	Course Outcomes	Design	, verify an	d implemen	t the function	ality of cou	inters.	
3	Aim	-			s (Synchrono , using Verilo		ıd Asynchro	onous reset)
4	Material / Equipment Required	Lab Ma	nual					
5	Theory, Formula, Principle, Concept	ъ Ч		OX 9(5 0)				
6	Procedure, Program, Activity, Algorithm, Pseudo Code		step 3: s step 4: c	vrite the prog ave the prog heck syntax	-	ors		

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7	Block, Model Reactio	Circuit, Diagram, n Equation, ed Graph	module bcd(rst,c input rst,clk; output reg[3:0 always@ begin if(rst) q=4' else beg q= i end endmodule			
8	Observ Table, Table, (Look-up	INPUT Rst Clk 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 1 X	OUTPUT Q 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 0000	• Truth table ve	rification
	Sample Calcula Graphs		Name Value ■ q[3:0] ↓ rst ↓ dk 1	20 ns 0000 X 000	140 ns 160 ns 1 X 0010 X 0011 X 0100 X 01	80 ns 100 ns 100 ns 100 ns 100 ns 1001
11	Results	& Analysis				

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12	Applica	tion Areas	Design of top level digital circuits.							
13	Remark	(S								
14	Faculty	Signature								
	with Da	ite								

Experiment 06 : Write HDL code to display messages on an alpha numeric LCD display

_	Experiment No.:	1	Marks		Date Planned	C	Date Conducte d	
1	Title	Write	HDL code t	to display me	essages on an a	Ipha num	eric LCD di	splay
2	Course Outcomes	Desig	n the digita	al system for	Interfacing FPC	A with He	x Keypad.	
3	Aim	Write	HDL code t	to display me	essages on an a	lpha num	eric LCD di	splay
4	Material / Equipment Required	Lab M	anual					
5	Theory, Formula, Principle, Concept							
6	Procedure, Program, Activity, Algorithm, Pseudo Code		step 3: s step 4: c step 5:if step 6:si	vrite progran ave the prog heck syntax error then c mulate the d PGA implem	orrect the errors	s		
	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	•						
8	Observation Table, Look-up Table, Output	•	Truth tab	le verificatio	n			
9	Sample Calculations							
10	Graphs, Outputs							
11	Results & Analysis							
12	Application Areas	Desig	n of top lev	vel digital cir	cuits.			
13	Remarks							
14	Faculty Signature with Date							

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Experiment 07 : Write HDL code to control speed, direction of DC and Stepper motor.

-	Experiment No.:	8	Marks		Date Planned		Date Conducte d	
1	Title	Write	HDL code t	o control spe	eed, directior	n of DC and	l Stepper mo	otor.
2	Course Outcomes	-	n the digita r using HDL	-	Controlling	the speed a	and direction	n of stepper
3	Aim	Write	HDL code t	o control spe	eed, directior	n of DC and	l Stepper mo	otor.
	Equipment Required		lanual					
5	Theory, Formula, Principle, Concept							
6	Procedure, Program, Activity, Algorithm, Pseudo Code		step 3: s step 4: c step 5:if step 6:si	rite program ave the prog heck syntax error then co mulate the d PGA impleme	ram prrect the err esign	ors		
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	•	- - -	P				
8	Observation Table, Look-up Table, Output	•	Truth tab	le verificatio	n			
9	Sample Calculations							
10	Graphs, Outputs							
11	Results & Analysis							
	Application Areas	Desig	n of top lev	el digital cir	cuits.			
	Remarks							
	Faculty Signature with Date							



Experiment 08 : Write HDL code to accept Analog signal, Temperature sensor and display the data on LCD or Seven segment display.

-	Experiment No.:	9	Marks		Date Planned		Date Conducte d		
1				•	nalog signal, gment display	•	ure sensor	and	display
2	Course Outcomes	Desig	n the digita	al system for	Interfacing F	PGA with t	emperature	sens	sor
3				•	nalog signal, jment display	•	ure sensor	and	display
	Material / Equipment Required Theory, Formula,	Lab M	anual						
	Principle, Concept								
6	Procedure, Program, Activity, Algorithm, Pseudo Code		step 3: s step 4: c step 5:if step 6:si	rite progran ave the prog heck syntax error then co mulate the d PGA implem	orrect the err lesign	ors			
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	•	-						
8	Observation Table, Look-up Table, Output	•	Truth tab	le verificatio	n				
9	Sample Calculations								
10	Graphs, Outputs								
	Results & Analysis								
	Application Areas	Desig	n of top lev	el digital cir	cuits.				
	Remarks								
14	Faculty Signature with Date								

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Experiment 10 : Write HDL code to generate different waveforms (Sine, Square, Triangle, Ramp etc.,) using DAC – change the frequency.

-	Experiment No.:	10	Marks		Date Planned		Date Conducte d	
1	Title			to generate g DAC - chan			(Sine, Square,	Triangle,
2	Course Outcomes	Study	of DAC and	generation of	different sig	nals using HI	DL.	
3	Aim			to generate 9 DAC - chan			(Sine, Square,	Triangle,
	Equipment Required		lanual					
5	Theory, Formula, Principle, Concept							
6	Procedure, Program, Activity, Algorithm, Pseudo Code		step 3: s step 4: c step 5:if step 6:si	rite program ave the progr heck syntax error then co mulate the de PGA impleme	ram prrect the e esign	rrors		
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph							
8	Observation Table, Look-up Table, Output	•	Truth tab	le verification	n			
9	Sample Calculations							
10	Graphs, Outputs							
11	Results & Analysis							
12	Application Areas	Desig	n of top lev	el digital circ	cuits.			
	Remarks							
14	Faculty Signature with Date							

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10	Title:	Со	urse Lab Ma	nual			Page:	Page: 45 / 51	
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-	Experiment No.:	10	Marks		Date		Date		
					Planned		Conduc d	te	
1	Title	Write	HDL code	to generate	different	waveforms		lare	Triangle
				g DAC – chan			(Jine, Jqu	arc	, mangic,
2	Course Outcomes			-	-		DL.		
		-		to generate				lare	Triangle
				g DAC – chan			(Sinc, Squ	iure	, mangre,
4			Manual	<i>j</i>		40.0			
	Equipment								
	Required								
5	Theory, Formula,								
	Principle, Concept								
6	Procedure,		step 1: s	tart					
	Program, Activity,		step 2: w	rite program	iming				
	Algorithm, Pseudo		step 3: s	ave the prog	ram				
	Code	•	step 4: c	heck syntax					
			step 5:if	error then co	orrect the e	errors			
			step 6:si	mulate the d	esign				
		•	step 7: F	PGA impleme	entation				
		•	step 8: s	top					
7	Block, Circuit,	•	-						
	Model Diagram,		-						
	Reaction Equation,	•	-						
	Expected Graph								
8	Observation	•	Truth tab	le verification	n				
	Table, Look-up								
	Table, Output								
9	Sample								
	Calculations								
-	Graphs, Outputs								
	Results & Analysis								
	Application Areas	Desi	gn of top lev	el digital cire	cuits.				
	Remarks								
14	Faculty Signature								

_	Experiment No.:	10	Marks	Date	Date	
				Planned	Conducte	

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Title			5			(Sine,	Square,	Triangle,
Course Outcomes	-		-	-		DL.		
	-		-		-		Square.	Triangle.
			-			. ,	. ,	_ ,
Material /	Lab N	/Ianual						
Equipment								
Required								
Theory, Formula,								
Principle, Concept								
Procedure,	•	step 1: s	tart					
Program, Activity,	•	step 2: w	rite progran	nming				
Algorithm, Pseudo	•	step 3: s	ave the prog	ram				
Code	•	-	-					
	•				errors			
	•	-		2				
	•	-	-	entation				
	•	step 8: s	top					
		-						
,		-						
-	•	-						
	•	Truth tab	le verificatio	n				
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-	. .	<u> </u>	1 1	•				
	Desig	jn of top lev	ei aigital cir	cults.				
Faculty Signature with Date								
	Title Course Outcomes Aim Material / Equipment Required Theory, Formula, Principle, Concept Procedure, Program, Activity, Algorithm, Pseudo Code Block, Circuit, Model Diagram, Reaction Equation, Expected Graph Observation Table, Look-up Table, Output Sample Calculations Graphs, Outputs Results & Analysis Application Areas Remarks Faculty Signature	RampCourse OutcomesStudyAimWrite RampAimWrite RampMaterial/ Lab MEquipmentRequiredITheory, Formula, Principle, Concept•Procedure, 	TitleWriteHDL code Ramp etc.,) usingCourse OutcomesStudy of DAC andAimWriteHDL code Ramp etc.,) usingMaterial/Lab ManualEquipment Required-Required-Theory, Formula, Procedure, Procedure, Algorithm, Pseudo Code-Codestep 1: s step 2: w step 3: sBlock,Circuit, Model-ModelDiagram, resution step 4: cBlock,Circuit, step 6:si step 6:siBlock,Circuit, resution step 8: sBlock,Circuit, resution step 6:si step 7: FSample Calculations-Calculations Graphs, Outputs-Results & Analysis Application AreasDesign of top lev RemarksFacultySignature	TitleWrite HDL code to generate Ramp etc.,) using DAC - chanCourse OutcomesStudy of DAC and generation ofAimWrite HDL code to generate Ramp etc.,) using DAC - chanMaterial/ Lab ManualEquipmentLab ManualRequired- chanTheory, Formula, Principle, Concept- step 1: startProcedure, Program, Activity, Algorithm, Pseudo Code- step 2: write programAlgorithm, Pseudo Code- step 3: save the prog step 3: save the prog step 5: if error then compared in the dom step 8: stopBlock, Circuit, Model Diagram, Reaction Equation, Table, Output-Reaction Equation, Table, Output-Sample Calculations-Graphs, Outputs Results & AnalysisDesign of top level digital cir RemarksFaculty Signature-	TitleWrite HDL code to generate different Ramp etc.,) using DAC - change the freeCourse OutcomesStudy of DAC and generation of different signation AimAimWrite HDL code to generate different freeAimWrite HDL code to generate different freeMaterial/ Lab ManualEquipment Required- change the freeProcedure, Procedure, Program, Activity, Algorithm, Pseudo Code- step 1: startProgram, Activity, Algorithm, Pseudo Code- step 3: save the program - step 3: save the program - step 5: if error then correct the design - step 7: FPGA implementation - step 8: stopBlock, Dobservation Table, Look-up Table, Output- Truth table verificationSample Calculations- Truth table verificationGraphs, Outputs- Results & AnalysisApplication Areas PacultyDesign of top level digital circuits.Remarks FacultySignature	Title Write HDL code to generate different waveforms Ramp etc.,) using DAC – change the frequency. Course Outcomes Study of DAC and generation of different signals using H Aim Write HDL code to generate different waveforms Ramp etc.,) using DAC – change the frequency. Material / Lab Manual Equipment Required // Lab Manual Frinciple, Concept • step 1: start Procedure, Procedure, Procedure, Code • step 2: write programming • step 3: save the program Algorithm, Pseudo Code • step 1: check syntax • step 5: fif error then correct the errors • step 6: simulate the design • step 7: FPGA implementation • step 8: stop Block, Circuit, • - Model Diagram, • - Expected Graph • Truth table verification Observation Table, Output • Truth table verification Graphs, Outputs Results & Analysis Pesign of top level digital circuits. Remarks Faculty Sign of top level digital circuits.	Title Write HDL code to generate different waveforms (Sine, Ramp etc) using DAC - change the frequency. Course Outcomes Study of DAC and generation of different signals using HDL . Aim Write HDL code to generate different waveforms (Sine, Ramp etc) using DAC - change the frequency. Material / Lab Manual Equipment Required Principle, Concept • step 1: start Procedure, • step 1: start Program, Activity, • step 3: save the program Algorithm, Pseudo • step 3: save the program Code • step 1: check syntax • step 5: if error then correct the errors • step 6: simulate the design • step 8: stop • step 8: stop Block, Circuit, • - Negection Equation, • • zep 8: stop • Block, Look-up • Table, Output • Sample Calculations Graphs, Outputs Results & Analysis Application Areas Design of top level digital circuits. Remarks Faculty Signature	d d Title Write HDL code to generate different waveforms (Sine, Square, Ramp etc) using DAC – change the frequency. Course Outcomes Study of DAC and generation of different signals using HDL . Aim Write HDL code to generate different waveforms (Sine, Square, Ramp etc) using DAC – change the frequency. Material / Lab Manual Equipment equired Procedure, • step 1: start Program, Activity, • step 3: save the program Algorithm, Pseudo • step 4: check syntax • step 5: ferror then correct the errors • step 6: simulate the design • step 7: FPGA implementation • step 8: stop Block, Circuit, • Reaction Equation, • Voted Graph • Truth table verification Table, Lobuput Sample Calculations Graphs, Outputs Results & Analysis Application Areas Design of top level digital circuits. Remarks Faculty Signature

-	Experiment No.:	10	Marks		Date Planned		Date Conducte d	
1	Title	Write	HDL code	to generate	e different	waveforms	(Sine, Squar	e, Triangle,
		Ramp	Ramp etc.,) using DAC – change the frequency.					

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		Study of DAC and generation of different signals using HE	
3	Aim	Write HDL code to generate different waveforms	(Sine, Square, Triangle,
		Ramp etc.,) using DAC – change the frequency.	
4	,	Lab Manual	
	Equipment		
	Required		
5	Theory, Formula,		
	Principle, Concept		
6	Procedure,	• step 1: start	
	Program, Activity,		
	Algorithm, Pseudo		
	Code	• step 4: check syntax	
		 step 5:if error then correct the errors 	
		step 6:simulate the design step 7: FBCA implementation	
		step 7: FPGA implementationstep 8: stop	
7	Block, Circuit,		
1	Model Diagram,	· -	
	Reaction Equation,	• -	
	Expected Graph		
8	Observation	Truth table verification	
	Table, Look-up		
	Table, Output		
9	Sample		
	Calculations		
10	Graphs, Outputs		
	Results & Analysis		
		Design of top level digital circuits.	
-	Remarks		
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Experiment 11 : Write HDL code to simulate Elevator operation.

-	Experiment No.:	1	Marks	Date Planned	Date Conducte d			
1	Title	Write	e HDL code	o simulate Elevator opera	tion.			
2	Course Outcomes	Desi	Design an Elevator					
3	Aim	Write	Vrite HDL code to simulate Elevator operation.					
4	Material /	Lab	Manual					
	Equipment							
	Required							

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5	Theory, Formula,	
	Principle, Concept	
6	Procedure,	• step 1: start
	Program, Activity,	step 2: write programming
	Algorithm, Pseudo	 step 3: save the program
	Code	 step 4: check syntax
		 step 5:if error then correct the errors
		 step 6:simulate the design
		 step 7: FPGA implementation
		• step 8: stop
7	Block, Circuit,	• -
	Model Diagram,	• –
	Reaction Equation,	• –
	Expected Graph	
8	Observation Table,	Truth table verification
	Look-up Table,	
	Output	
9	Sample	
	Calculations	
10	Graphs, Outputs	
11	Results & Analysis	
12	Application Areas	Design of top level digital circuits.
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APPENDIX-1 DETAILED PROCEDURE FOR PROGRAM EXECUTION

Procedure To Work With Xilinx Tool :

To Create A Project

- 1. Double Click On XILINX ISE Icon
- 2. In ise project navigator window go to file and click on new project
- 3. Give any project name and note down the path, click next
- 4. Select spartan6 in family field and click next

To write HDL code

- 1. go to hierarchy window
- 2. right click on XC6SLX4-3TQC144
- 3. click on new source
- 4. select vhdl or verilog module
- 5. give file name without space and note down the path, click next
- 6. give name to input and output varible and click next
- 7. click on finish
- 8. type the program in editor window and save it
- 9. select the file hierarchy window
- 10. go to process window and click on synthesize- xst

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11. double click on check syntax

12. to check syntax error click on console if any error is present click on particular error and fix

the error

To Check Simulation Result

- 1. Select Simulation
- 2. Select Program In Hierarchy Window
- 3. Open Isim Simulator In Process Window
- 4. Double Click On Simulate Behavioral Model
- 5. Simulation Window Will Open
- 6. Right Click On Input(At A Time One Input)
- 7. Click On Force Constant
- 8. Enter The Input Value In ''force To Value'' Field
- 9. Apply And Then Ok
- 10. Repeat Steps 6 To 9 For All Inputs
- 11. In Time Period Field Make It To 1 second
- 12. Click On Run For The Time Specified On Toolbar
- 13. Verify The Simulation Results With Truth Table

Procedure To Download Onto Fpga:

Procedure For Creating A Bit File

- 1. Only One Program Should Be Available In Hierarchy Window
- 2. Select File (program)
- 3. Go To User Constraints In Process Window
- 4. Double Click On I/O Pin Planning (plan Ahead) Pre-Sysnthesis
- 5. Click On Yes
- 6. In I/O Ports Window Open Scalar Ports
- 7. I/O Port Properties Window Should Be Opened
- 8. Click On Site And
- 9. Enter The Pin No (provided By Vendor) Example: P124- And Click On Apply

(assigning Pin Will Be Done For All Inputs And Outputs)

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- 10. Click On Save
- 11. Ucf File Will Be Created In Hierarchy Window
- 12. In Process Window Double Click On Design: Generate Programming File
- 13. In Process Window Double Click On Configure Target Device->Ok
- 14. Bit File Will Be Generated

Procedure For Dumping Bit File On To The FPGA Kit

- 1. Double Click On Vsf-6-2.0(Present On Desktop)
- 2. Check Com Port Number (right Click My Computer-->Manage-->Device
- Manager-->Open Ports(Com&Lpt))
- 3. Select Particular Com Port Number
- 4. In VSF-6-2.0 Window Select File And Click On Load File
- 5. Select The Particular Bit File And Click On Open
- 6. Click On Configure File
- "FPGA Programmed Successfully" Will Be Displayed
- 7. Verify The Results With Truth Table